

**LIMITED SWITCH DYNAMIC LOGIC CIRCUIT WITH KEEPER****ABSTRACT OF THE DISCLOSURE**

5 An LSDL circuit has both an output and a complementary output generated by inverting the output with an inverter logic gate. A keeper PFET is added by coupling its drain terminal to the dynamic node. The keeper PFET has its source terminal coupled to the positive power supply voltage and its gate terminal coupled to the complementary output. The output and the dynamic node may both be at a logic one when the output is a logic one from the previous evaluation cycle and the dynamic node is precharged. In this case, the complementary output is a logic zero which  
10 turns ON the keeper PFET and reinforces the precharge on the dynamic node. When the output is evaluating to a logic zero, the output will transition quickly to a logic zero. If the output is transitioning from a logic zero to a logic one, then the keeper PFET is OFF and does not affect the dynamic node.